PENDING CLAIMS:

1. (Original) An integrated circuit comparator comprising:

an input receiving an input signal representative of a difference between quantities to be compared; and

an input gain stage receiving the input signal and biased with a pulsed bias current, the input gain stage producing a gain based upon the input signal.

2. (Original) The integrated circuit comparator according to claim 1, wherein the input signal is a current representative of transconductance of a differential pair of input transistors.

3. (Original) The integrated circuit comparator according to claim 1, wherein the input gain stage further comprises a current source biased by the pulsed bias current and controlled by the input signal.

4. (Previously Presented) The integrated circuit comparator according to claim 1, further comprising:

a voltage limiter and a hysteresis circuit coupled to an output of the input gain stage to reduce spurious output transitions when the pulsed bias current changes state.

5. (Previously Presented) The integrated circuit comparator according to claim 4, further comprising:

an output gain stage coupled to the hysteresis circuit and having a gain varying with the bias change of the input gain stage.

6. (Original) The integrated circuit comparator according to claim 4, further comprising:

an output gain stage coupled to the hysteresis circuit and having a fixed gain and a propagation delay negligible with respect to a propagation delay of the input gain stage.

7. (Original) The integrated circuit comparator according to claim 1, wherein the pulsed bias current comprises a pulse at one edge of a system clock and an output of the comparator is sampled at another edge of the system clock.

8. (Previously Presented) The integrated circuit comparator according to claim 1, wherein the comparator selectively operates in a first mode in which the input gain stage is biased by a bias current with a defined first level value or in a second mode in which the input gain stage is biased by a bias current with a different second level value.

9. (Original) A method of operating an integrated circuit comparator comprising:

receiving an input signal representative of a difference between quantities to be compared at an input for the comparator; and

transmitting the input signal from the input to an input gain stage biased with a pulsed bias current, the input gain stage producing a gain based upon the input signal.

10. (Original) The method according to claim 9, wherein the input signal is a current representative of transconductance of a differential pair of input transistors.

11. (Original) The method according to claim 9, wherein the input gain stage further comprises a current source biased by the pulsed bias current and controlled by the input signal.

12. (Previously Presented) The method according to claim 9, further comprising:

with an output signal from the input gain stage, driving a voltage limiter and a hysteresis circuit coupled to the output of the input gain stage to reduce spurious output transitions when the pulsed bias current changes state.

13. (Original) The method according to claim 12, further comprising:

varying a gain of an output gain stage coupled to the hysteresis circuit with the bias change of the input gain stage.

14. (Original) The method according to claim 12, further comprising:

fixing a gain of an output gain stage coupled to the hysteresis circuit and having a propagation delay negligible with respect to a propagation delay of the input gain stage.

15. (Original) The method according to claim 9, wherein the pulsed bias current comprises a pulse at one edge of a system clock and an output of the comparator is sampled at another edge of the system clock.

16. (Original) The method according to claim 9, wherein the comparator selectively operates in a first mode in which the input gain stage is biased by a continuous bias current or in a second mode in which the input gain stage is biased by the pulsed bias current.

17. (Original) An integrated circuit comprising:

a comparator selectively operating in a first mode in which an input gain stage of the comparator is biased with a pulsed bias current and a second mode in which the input gain stage is biased with a continuous bias current.

18. (Original) The integrated circuit according to claim 17, wherein the input gain stage receives an input signal representative of a difference between quantities to be compared and produces a gain based upon a current for the input signal representative of transconductance of a differential pair of input transistors.

19. (Previously Presented) The integrated circuit according to claim 18, wherein the input gain stage further comprises a current source producing the pulsed or continuous bias current and controlled by the input signal.

20. (Previously Presented) The integrated circuit according to claim 19, further comprising:

a voltage limiter and a hysteresis circuit coupled to an output of the input gain stage to reduce spurious output transitions when the pulsed bias current changes state.